XIN CORE TECHNOLOGY

X32F1003xx
ARM® Cortex™-M3 32-bit MCU

Datasheet

Table of Contents

1 General description

The X32F1003xx device is a 32-bit general-purpose microcontroller based on the ARM® Cortex™-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex™-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The X32F1003xx device incorporates the ARM® Cortex™-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1 MB on-chip Flash memory and up to 32 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer 12-bit ADCs, 12-bit DACs, general-purpose 16-bit timers, basic timers plus two PWM advanced-control timer, as well as standard and advanced communication interfaces: SPI, I^2C, UART, USB 2.0 FS, and CAN.

The device operates from a 2.5 to 5.0 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the X32F1003xx devices suitable for a wide range of applications, especially in areas such as industrial control, inventer, consumer and POS, vehicle GPS, toy controller and so on.

2 Device overview

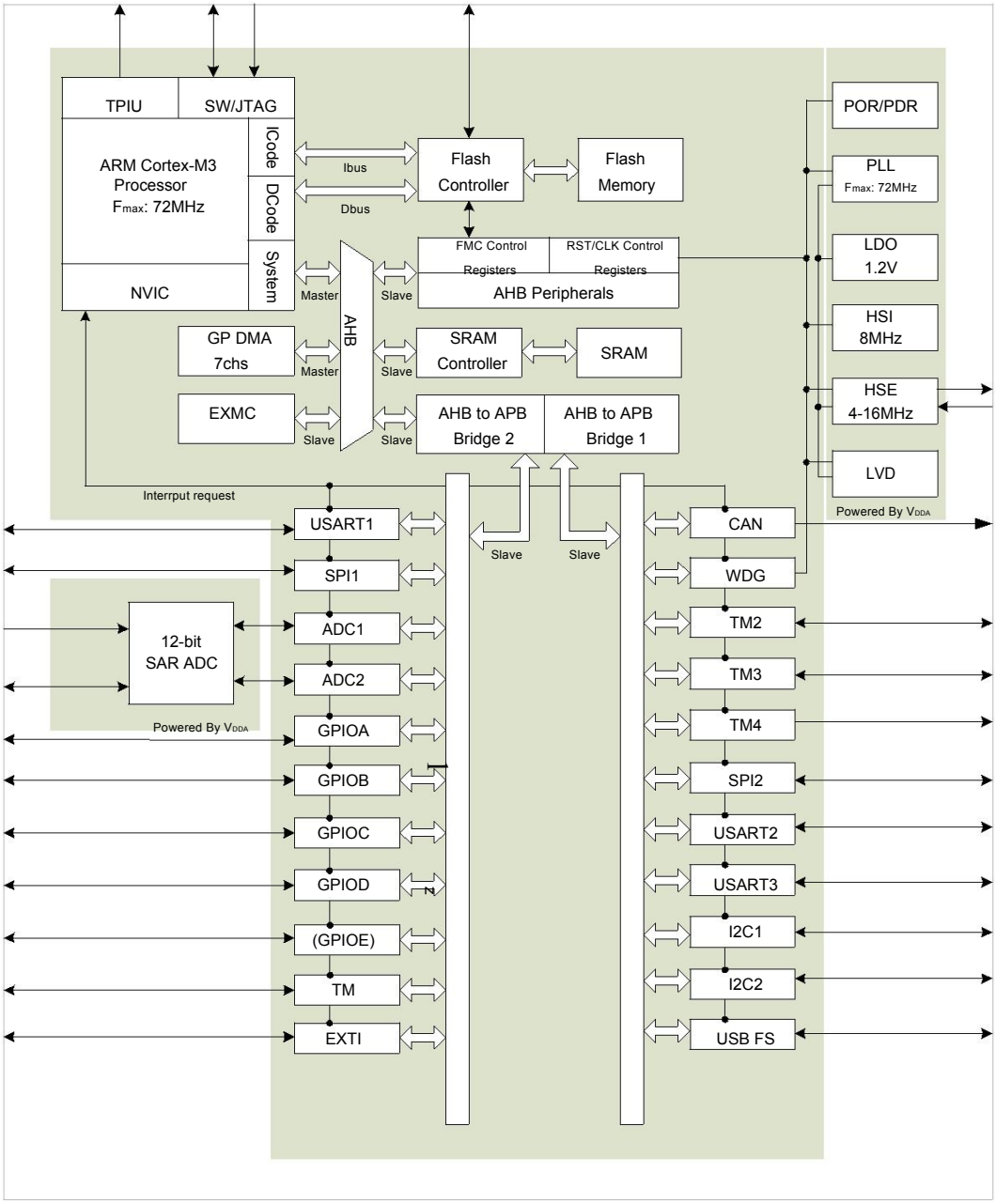
2.1 Device information

Table 1. X32F1003xx devices features and peripheral list

Part Number		X32F1003XX							
		T4	T6	T8	TB	C4	C6	C8	CB
Flash (KB)		128	256	512	1024	128	256	512	1024
SRAM (KB)		32	32	32	32	32	32	32	32
Timers	GPTM	2	2	2	2	2	2	2	2
	Advanced TM	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1
Connectivity	USART	2	2	2	2	2	2	2	2
	I2C	2	2	2	2	2	2	2	2
	SPI	2	2	2	2	2	2	2	2
	CAN 2.0B	1	1	1	1	1	1	1	1
	USB 2.0 FS	1	1	1	1	1	1	1	1
GPIO		37	37	37	37	26	26	26	7
DAC		1	1	1	1	1	1	1	1
EXTI		16	16	16	16	16	16	16	16
ADC	Units	2	2	2	2	2	2	2	2
	Channels	16	16	16	16	10	10	10	10
Package		LQFP64				LQFP48			

2.2 Block diagram

Figure 1. X32F1003xx block diagram



2.3 Pinouts and pin assignment

Figure 2. X32F1003Rx LQFP64 pinout

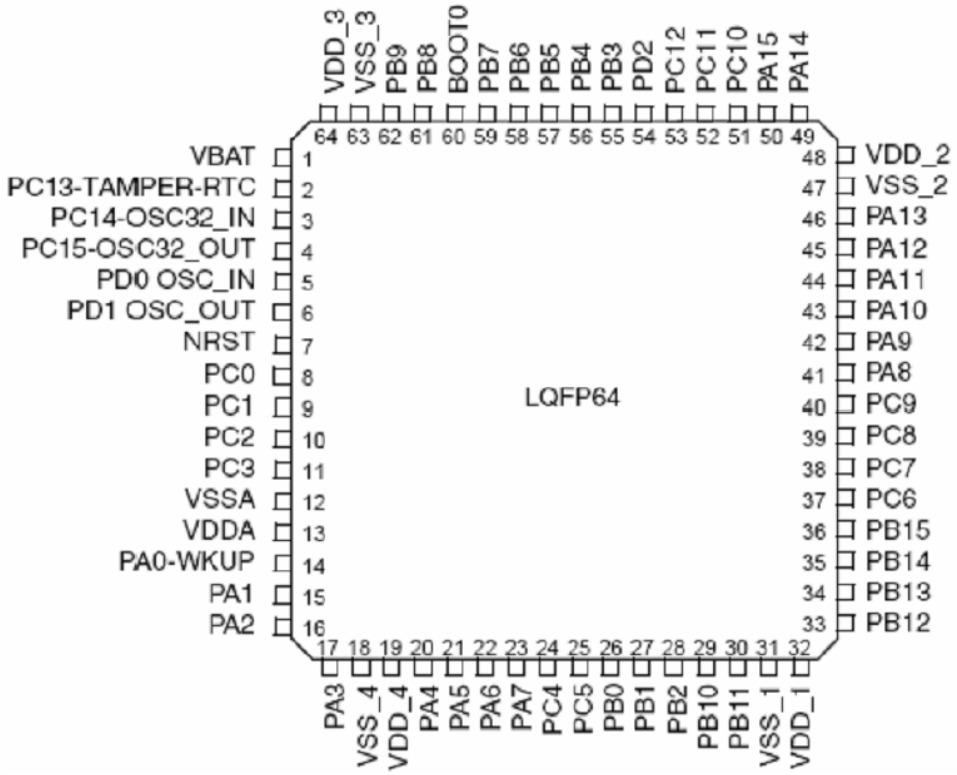
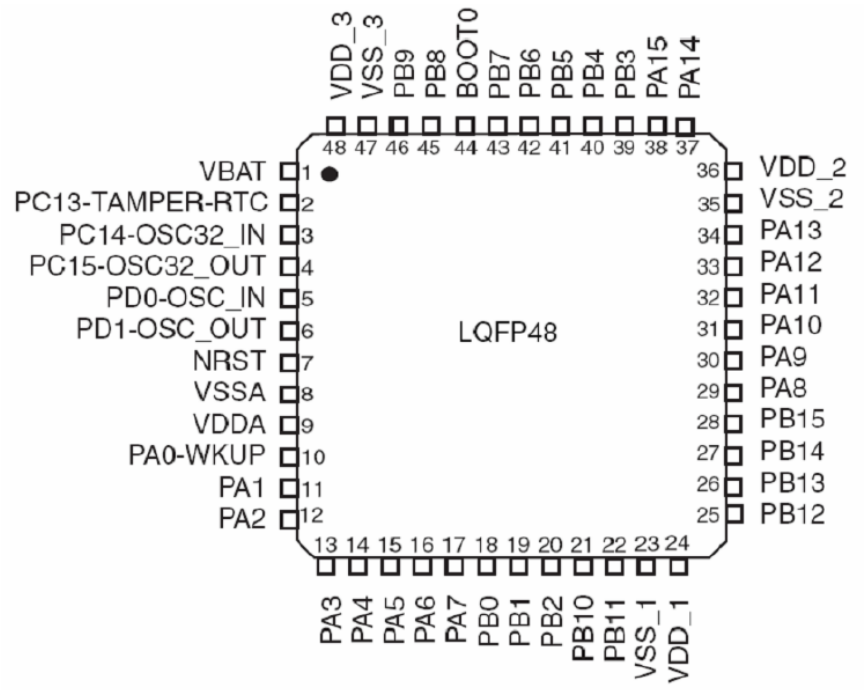
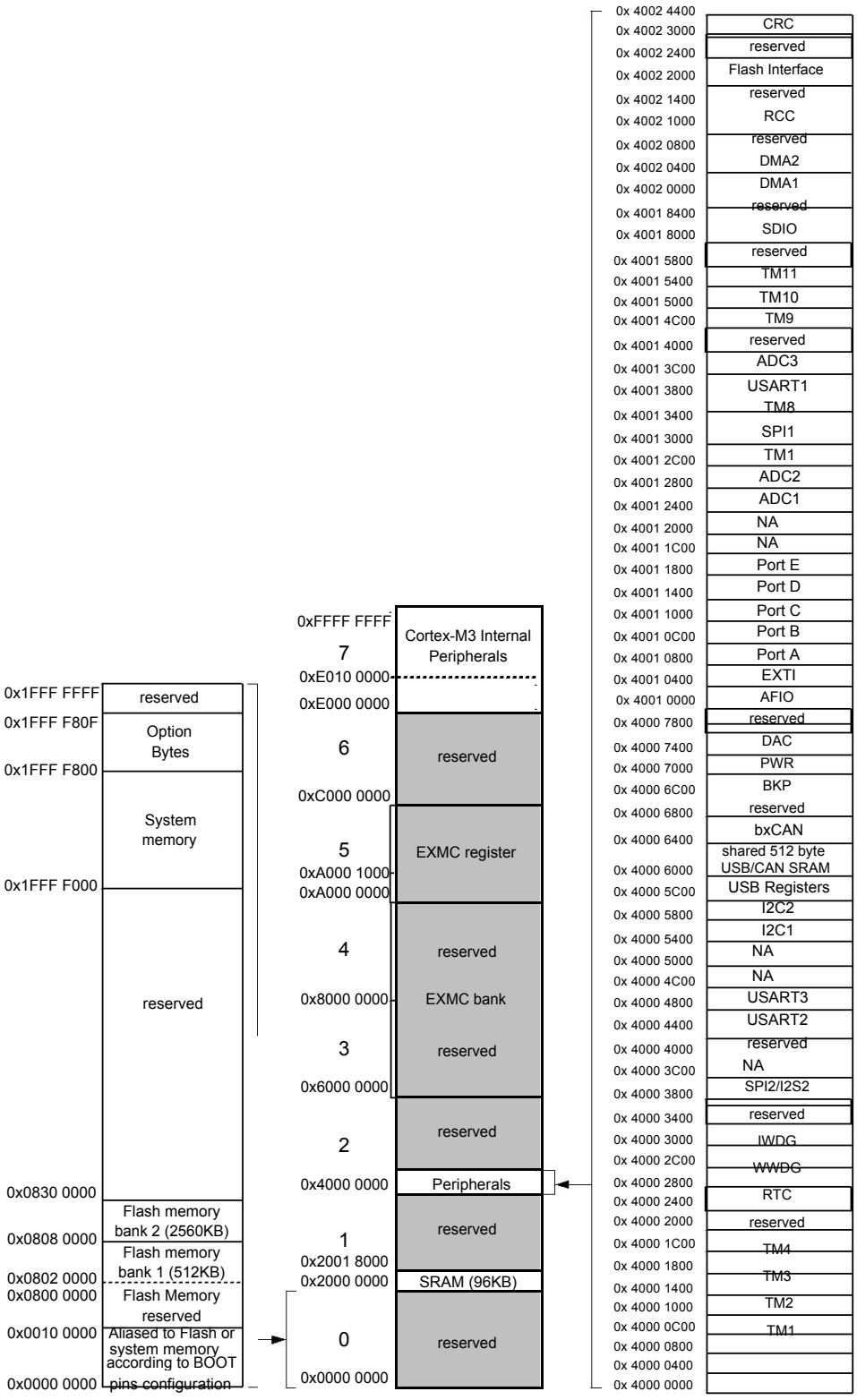


Figure 3. X32F1003Rx LQFP48 pinout



2.4 Memory map

Figure 4. X32F1003xx memory map



2.5 64 Pin definition

Table 2. X32F1003xx 64 pin definition

Pin number	Pins	Type	function	Default	Alternate
1	VBAT	S	VBAT		
2	PC13-TAMPER-RTC	I/O	PC13	TAMPER-RTC	
3	PC14-OSC32_IN	I/O	PC14	OSC32_IN	
4	PC15-OSC32_OUT	I/O	PC15	OSC32_OUT	
5	OSC_IN	I	OSC_IN	PD0	CAN_RX
6	OSC_OUT	O	OSC_OUT	PD1	CAN_TX
7	NRST	I/O	NRST		
8	PC0	I/O	PC0	ADC2_IN2	
9	PC1	I/O	PC1	ADC2_IN3	
10	PC2	I/O	PC2	ADC2_IN4	
11	PC3	I/O	PC3	ADC2_IN5	
12	VSSA	S	VSSA		
13	VDDA	S	VDDA		
14	PA0-WKUP	I/O	PA0	ADC1_IN0/COMP1_INP0/ COMP1_INM6/COMP2_INP0/ WKUP/UART2_CTS/ TIM2_CH1_ETR	
15	PA1	I/O	PA1	ADC1_IN1/COMP1_INP1/ COMP2_INP1/OPAMP1_INP1/ OPAMP1_INM1/OPAMP2_INM3/ OPAMP3_INP2/OPAMP3_INM2/ UART2_RTS/TIM2_CH2	
16	PA2	I/O	PA2	ADC1_IN2/COMP1_INP2/ COMP2_INP2/COMP2_INM6/ UART2_RX/TIM2_CH3	
17	PA3	I/O	PA3	ADC1_IN3/COMP1_INP3/ COMP2_INP3/OPAMP1_INP2/ OPAMP1_INM2/OPAMP2_INM2/ OPAMP3_INP0/ UART2_RX/TIM2_CH4	

18	VSS_4	S	VSS_4		
19	VDD_4	S	VDD_4		
20	PA4	I/O	PA4	ADC1_IN4/DAC1_OUT/ COMP1_INP4/COMP1_IN M4/ COMP2_INP4/COMP2_IN M4/ OPAMP2_INP3/OPAMP3_ INM1/ OPAMP4_INM0/OPAMP4_ INP1/ SPI1_NSS	
21	PA5	I/O	PA5	ADC1_IN5/DAC2_OUT/ COMP1_INP5/COMP1_IN M5/ COMP2_INP5/COMP2_IN M5/ OPAMP1_INP1/OPAMP1_ INM1/ OPAMP2_INP0/OPAMP2_ INM1/ OPAMP3_INM0/OPAMP3_ INP1/ OPAMP4_INM1/SPI1_SCK	
22	PA6	I/O	PA6	ADC1_IN6/COMP1_INP6/ COMP1_INM7/COMP2_IN P6/ COMP2_INM7/OPAMP4_I NM2/ SPI1_MISO/TIM3_CH1	TIM1_BKIN
23	PA7	I/O	PA7	ADC1_IN7/COMP1_INP7/ COMP2_INP7/OPAMP1_I NP0/ OPAMP1_INM0/OPAMP4_ INM3/ SPI1_MOSI/TIM3_CH2	TIM1_CH1N
24	PC4	I/O	PC4	ADC2_IN6/OPAMP4_INP0	
25	PC5	I/O	PC5	ADC2_IN7/OPAMP2_INM0	
26	PB0	I/O	PB0	ADC2_IN0/OPAMP2_INP1 / OPAMP3_INP3/OPAMP3_ INM3/ OPAMP4_INP2/ TIM3_CH3	TIM1_CH2N
27	PB1	I/O	PB1	ADC2_IN1/OPAMP2_INP2 / OPAMP4_INP3/ TIM3_CH4	TIM1_CH3N
28	PB2	I/O	PB2/BOO		

			T1		
29	PB10	I/O	PB10	I2C2_SCL/UART3_TX/	TIM2_CH3
30	PB11	I/O	PB11	I2C2_SDA/UART3_RX	TIM2_CH4
31	VSS_1	S	VSS_1		
32	VDD_1	S	VDD_1		
33	PB12	I/O	PB12	SPI2_NSS/TIM1_BKIN/	
34	PB13	I/O	PB13	SPI2_SCK/UART3_CTS/ TIM1_CH1N	
35	PB14	I/O	PB14	SPI2_MISO/UART3_RTS/ TIM1_CH2N	
36	PB15	I/O	PB15	SPI2_MOSI/TIM1_CH3N/	
37	PC6	I/O	PC6		TIM3_CH1
38	PC7	I/O	PC7		TIM3_CH2
39	PC8	I/O	PC8		TIM3_CH3
40	PC9	I/O	PC9		TIM3_CH4
41	PA8	I/O	PA8	TIM1_CH1/MCO	
42	PA9	I/O	PA9	UART1_TX/TIM1_CH2	
43	PA10	I/O	PA10	UART1_RX/TIM1_CH3/	
44	PA11	I/O	PA11	UART1_CTS/USBDM/CAN _RX/ TIM1_CH4	
45	PA12	I/O	PA12	UART1_RTS/USBDP/CAN _TX/ TIM1_ETR	
46	PA13	I/O	JTMS/SW DIO		PA13
47	VSS_2	S	VSS_2		
48	VDD_2	S	VDD_2		
49	PA14	I/O	JTCK/SW CLK		PA14
50	PA15	I/O	JTDI		PA15/TIM2_C H1_ETR/ SPI1_NSS

51	PC10	I/O	PC10		UART3_TX
52	PC11	I/O	PC11		UART3_RX
53	PC12	I/O	PC12		
54	PD2	I/O	PD2	TIM3_ETR	
55	PB3	I/O	JTDO		PB3/TRACES WO/ TIM2_CH2/SPI 1_SCK
56	PB4	I/O	NJTRST		PB4/TIM3_CH 1/ SPI1_MISO
57	PB5	I/O	PB5		TIM3_CH2/SPI 1_MOSI
58	PB6	I/O	PB6	I2C1_SCL/TIM4_CH1/	UART1_TX
59	PB7	I/O	PB7	I2C_SDA/TIM4_CH2	UART1_RX
60	BOOT0	I	BOOT0		
61	PB8	I/O	PB8	TIM4_CH3	I2C1_SCL/CAN_RX
62	PB9	I/O	PB9	TIM4_CH4	I2C1_SDA/CAN_TX
63	Vss_3	S	Vss_3		
64	Vdd_3	S	Vdd_3		

3 Functional description

3.1 ARM® Cortex™-M3 core

The Cortex™-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex™-M3 processor core
- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex™-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 1024 Kbytes of Flash memory
- Up to 32 Kbytes of SRAM

The ARM® Cortex™-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner Flash and 32 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The Figure 6. X32F1003xx memory map shows the memory map of the X32F1003xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 16 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32 KHz crystal oscillator
- Integrated system clock PLL
- 2.5 to 5.0 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. See Figure 7 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.5 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.5 to 5V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.5 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 2.5 to 3.6 V, power supply for RTC, external clock 32.768 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART1 in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 1 of Flash memory is selected. It also supports to boot from bank 2 of Flash memory by setting a bit in option bytes.

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (HSI, HSE) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the HSI is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of HSI, HSE and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the IWDG reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
- Conversion range: V_{SSA} to V_{DDA} (0 to 1.2 V)
- Temperature sensor

Up to three 12-bit 1 μs multi-channel ADCs are integrated in the device. Each is a total of up to 21 multiplexed external channels. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADCs can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timers (TM1) with internal connection. The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 0 V to 1.2 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.7 Digital to analog converter (DAC)

- 12-bit DAC converters of independent output channel
- 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channels are used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+}.

3.8 DMA

- 7 channel DMA 1 controller and 5 channel DMA 2 controller
- Peripherals supported: Timers, ADC, SPIs, I^2Cs, USARTs and DAC

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Four types of access method are supported: peripheral to peripheral, peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 40 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 40 general purpose I/O pins (GPIO) in X32F1003xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC12, to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10 Timers and PWM generation

- One 16-bit advanced-control timer (TM1)
- Up to 4 independent channels of PWM, output compare or input capture for each GPTM and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Independent watchdog and window watchdog)

The advanced-control timer (TM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned counting modes)
- Single pulse mode output

If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), known as TM2 ~ TM5 can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM6 is mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The X32F1003xx have two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in

debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode, 400 kHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time.

3.13 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs
- Supports both asynchronous and clocked synchronous serial communication modes

The USART(USART1, USART2 and USART3) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver.

3.15 Universal serial bus full-speed (USB 2.0 FS)

- One full-speed USB Interface with frequency from 1.5Mbit/s to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between one or more devices. Full-speed peripheral is compliant with the USB 2.0 specification. The device controller enables 12 Mbit/s data exchange with a USB Host controller. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.16 Controller area network (CAN)

- One CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 14 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.17 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.18 Package and operation temperature

- LQFP64 (X32F1003 Rx), LQFP48 (X32F1003 Cx)
- Operation temperature range: -40°C to +85°C (industrial level)

4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{SS} + 5	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2 Recommended DC characteristics

Table 3. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{BAT}=3.3V, HSE=8MHz, System clock=108 MHz, All peripherals enabled	—	45.2	—	mA
		V_{DD}=V_{BAT}=3.3V, HSE=8MHz, System clock =108 MHz, All peripherals disabled	—	36.0	—	mA
		V_{DD}=V_{BAT}=3.3V, HSE=8MHz, System clock =72MHz, All peripherals enabled	-—	32.4	—	mA
		V_{DD}=V_{BAT}=3.3V, HSE=8MHz, System Clock =72 MHz, All peripherals disabled	—	26.1	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{BAT}=3.3V, HSE=8MHz, CPU clock off, All peripherals enabled	—	23.2	—	mA
		V_{DD}=V_{BAT}=3.3V, HSE=8MHz, CPU clock off, All peripherals disabled	—	13.9	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{BAT}=3.3V, All clock off, LSI on, RTC on, All GPIOs analog mode	—	0.91	1.4	mA
	Supply current (Standby mode)	V_{DD}=V_{BAT}=3.3V, LDO off, LSE off, LSI on, RTC on	—	24.5	—	μA
I_{BAT}	Battery supply current (Standby mode)	V_{DD} not available, V_{BAT}=3.3V, LDO off, LSE on, LSI off, RTC on	—	13.1	—	μA
		V_{DD} not available, V_{BAT}=3.3 V, LDO off, LSE off, LSI on, RTC on	—	10.8	—	M A

4.4 External clock characteristics

Table5. High speed external clock (HSE) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High Speed External oscillator (HSE) frequency	V_{DD}=3.3V	4	8	16	MHz
C_{HSE}	Recommended load capacitance on OSC_IN and OSC_OUT		—	20	30	pF
D_{HSE}	HSE oscillator duty cycle		48	50	52	%
I_{DDHSE}	HSE oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1.4	—	µA
t_{SUHSE}	HSE oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 6. Low speed external clock (LSE) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low Speed External oscillator (LSE) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	1000	KHz
C_{LSE}	Recommended load capacitance on OSC32_IN and OSC32_OUT		—	—	15	pF
D_{LSE}	LSE oscillator duty cycle		48	50	52	%
I_{DDLSE}	LSE oscillator operating current	V_{DD}=V_{BAT}=3.3V	—	1.4	—	µA
t_{SULSE}	LSE oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	3	—	s

4.5 Internal clock characteristics

Table 7. High speed internal clock (HSI) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	High Speed Internal Oscillator (HSI) frequency	V_{DD}=3.3V, T_A=-40°C ~+85°C	—	8	—	MHz
ACC_{HSI}	HSI oscillator Frequency accuracy	Factory-trimmed V_{DD}=3.3V, T_A=25°C	+1	—	-1	%
D_{HSI}	HSI oscillator duty cycle	V_{DD}=3.3V, f_{HSI}=8MHz	48	50	52	%
I_{DDHSI}	HSI oscillator operating current	V_{DD}=3.3V, f_{HSI}=8MHz	—	80	100	μA
t_{SUHSI}	HSI oscillator startup time	V_{DD}=3.3V, f_{HSI}=8MHz	1	—	2	us

Table 13. Low speed internal clock (LSI) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal oscillator (LSI) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	30	40	60	KHz
I_{DDLSI}	LSI oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	1	2	μA
t_{SULSI}	LSI oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	—	80	μs

4.6 PLL characteristics

Table 8. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency		1	8	25	MHz
f_{PLL}	PLL output clock frequency		16	—	72	MHz
t_{LOCK}	PLL lock time		—		100	μs

4.7 Memory characteristics

Table 9. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	Us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	Ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	S

4.8 GPIO characteristics

Table 10. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	V_{DD}=2.6V	-0.3	—	0.9	V
V_{IH}	High level input voltage	V_{DD}=2.6V	1	—	5.5	V
V_{OL}	Low level output voltage	V_{DD}=2.6V	—	—	0.2	V
V_{OH}	High level output voltage	V_{DD}=2.6V	2.3	—	—	V
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

4.9 ADC characteristics

Table 11. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{ADCIN}	ADC input voltage range		0	—	V_{REF+}	V
f_{ADC}	ADC clock		0.6	—	14	MHz
f_S	Sampling rate		—	—	1	MHz
$f_{ADCCONV}$	ADC conversion time	f_{ADC}=14MHz	1	—	18	μs
R_{ADC}	Input sampling switch resistance		—	—	1	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	32	—	pF
t_{SU}	Startup time		—	—	1	μs

4.10 DAC characteristics

Table 12. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{DACIN}	DAC input voltage range		0	—	V_{REF+}	V
R_{LOAD}	Load resistance	Resistive load vs. V_{SSA} with buffer ON	5	—	—	kΩ
C_{LOAD}	Load capacitance	No pin/pad capacitance included	—	—	50	pF
DNE	Differential non-linearity error	DAC in 12-bit	—	—	±3	LSB
INL	Integral non-linearity	DAC in 12-bit	—	—	±5	LSB
Offset	Offset error	DAC in 12-bit, V_{REF+} = 3.6 V	—	—	±12	LSB
GE	Gain error	DAC in 12-bit	—	—	±0.5	%

4.11 I2C characteristics

Table 13. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{SCL(H)}$	SCL clock high time		4.0	—	0.6	—	ns
$t_{SCL(L)}$	SCL clock low time		4.7	—	1.3	—	ns

4.12 SPI characteristics

Table 14. SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	18	MHz
$t_{SCK(H)}$	SCK clock high time		19	—	—	ns
$t_{SCK(L)}$	SCK clock low time		19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time		—	—	25	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time		3	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

5 Package information

5.1 LQFP package outline dimensions

Figure 5. LQFP package outline

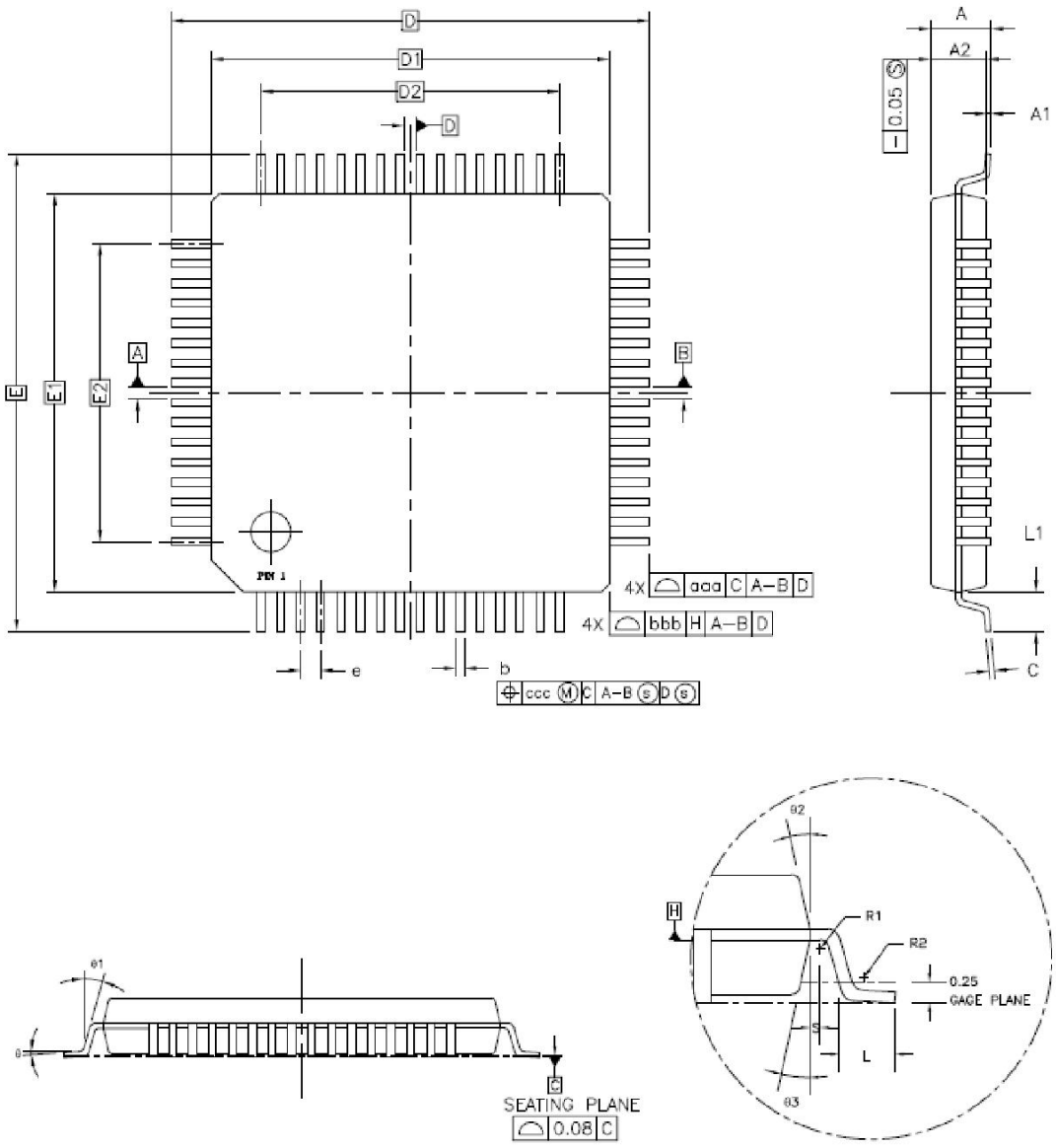


Table 15. LQFP package dimensions

Symbol	LQFP48			LQFP64		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15
A2	0.95	1.00	1.05	1.35	1.40	1.45
D	-	9.00	-	-	12.00	-
D1	-	7.00	-	-	10.00	-
E	-	9.00	-	-	12.00	-
E1	-	7.00	-	-	10.00	-
R1	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-
b	0.17	0.22	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-
D2	-	17.50	-	-	17.50	-
E2	-	17.50	-	-	17.50	-
aaa	0.20			0.20		
bbb	0.20			0.20		
ccc	0.08			0.08		

(Original dimensions are in millmeters)

6 Revision History

Table 16. Revision history

Revision No.	Description	Date
0.2	Add characteristics part	Aug.28, 2015